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Design of Hybrid Cmos-Set Based Hamming Code Nano Ic

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ABSTRACT: *'e-beam' Lithography technique is a boon to the device engineers. Consequently, Single Electronic Transistors (SET), a rather new field of solid state science and technology fostered promptly in both theory and experiments. Exploration in this arena ushered promising domino effect for post CMOS era devices. In spite of copious pros of SET, the delicacy in fully exploring the 'material goods' of SET and further deploying them in new architectures to integrate them on a single chip remains a challenge. The fragilities are room temperature operation, low gain and background charges. Since then, un-put-down-able device scientists articulated hybridization of existing CMOS technology with SETs to incapacitate the listed drawbacks of SET. This has reconnoitered new skyline in device research and was referred as Hybrid CMOS-SET. Here the authors pen down a comparable attempt to attain hybrid CMOS-SET based Error free Communication nano IC based on the orthodox theory of Hamming Code. P-Spice simulation software is used to study the robustness and fastness of the novel architecture by equating it with existing CMOS technology.*

Keywords: *CMOS, Hamming Code, Lithography technique, Nano IC, Robustness, SET*

I. INTRODUCTION

Assurance of maximum integration density and least power consumption is ensured in Single Electron Transistor like devices [1]. Subsequently Researchers invested high quality time since the last decade to cognize the functioning of this new aspiring post CMOS contender in the low power VLSI vicinity. The relevance of Single Electron Transistor (SET) is included for charge sensing applications like readout of electron memories and charge coupled devices, in metrology and in other precession measurement [2]. SET is quite esteemed among all post CMOS nm devices due to its particular electrical characteristics, simplicity and robustness. Furthermore SETs are elements of nanometer scale electronics as they can perceive the motion of individual electrons. Two distinctive area of SET research flourished concurrently- SET fabrication and SET logical realization. For the later part different meticulous simulators for the precise simulation of SET are introduced alike SIMON [3], KOSEC and MOSES. These all simulators are fastidious but the delicacy is that they involve rigorous computations and they are highly time consuming. Conceptually, maneuver of SET relies upon the transfer of discrete electron through the channel after tunneling through the Coulomb Blockade region. Accordingly SET possess atypical attributes like periodically increasing and decreasing of drain current vis-à-vis gate voltage [4]. To yield the utmost benefit of this unique feature- exploring its conduct in circuit behavioral is essential i.e., whether the circuit is fully operational or not with low power consumption than earlier nm MOSFET devices. Empirical research revealed mammoth success in achieving the heights of nm scale device designing using SET. Accordingly, SET resembles significant gain over MOSFET i.e. low power consumption, high speed, and merely one or very few electrons are required to process one bit of information. However SET is not flawless, its demerits are low current drive, background charge effect and lacks of room temperature realization, besides SETs are sensitive to random background charges and it has very high output impedance. Sincere efforts are reported currently to overcome the drawback of room temperature operable technology and Researchers have invented room temperature operable SET [6]. Because of these limitations the SET has to undergo farthest research before its commercial outcome.

On the other hand MOSFET have high gain and current drive, possess much matured fabrication technology and can be operated in room temperature. Thus it can compensate the drawbacks of SET. Thus the cultivation of hybridizing both SET and CMOS appeared and attracted Researchers worldwide and a new device draw the attention of the researchers: Hybrid SET-CMOS, which comprises of the advantages of SET and CMOS [7]. This new innovation Hybrid CMOS-SET combines new transport functionalities of electron which leads to better device designing and manufacturing. The authors here render Hybrid CMOS SET based nano IC that is to be incorporated in future communication system.

II. HYBRID CMOS-SET CO-INTEGRATION

Single electron transmission gate equivalent circuit is deliberated by Yukinon Ono et al [7] along with other SET-MOS quaternary transmission gate [8]. The metaphor of the proposed Hybrid CMOS-SET

Transmission gate is rendered in fig. 1. Corresponding hybrid circuits are constructed one after another. It comprises of a pull-up / pull-down control circuit following an electrical switch. It increases the switching speed, gate fan-out and overall working ominously [9,10]. Basically a SET and an nMOS transistor is coupled in parallel to formulate the Hybrid CMOS-SET circuit wich is controlled by a complementary switching signals. Here the switch is closed when A = 1 and opened when A=0. Thereby the output Y = A.X

$$Y = \begin{cases} 0 & if \quad A=0 \\ x & if \quad A=1 \end{cases}$$

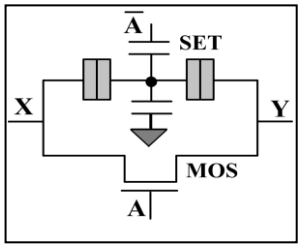

Fig.1: Basic structure of SET-MOS hybrid logic

III. CIRCUIT DESIGN

Fig. 2 is a Hybrid CMOS-SET based Hamming Code Circuit. Elementary research was carried in Delft University in Netherlands where Researchers developed a SPICE based SET circuit simulation package [11] using the Orthodox theory of Hybrid CMOS-SET. Here the authors exclusively adhered to the same model and the circuit was simulated using PARTSIM Simulator.

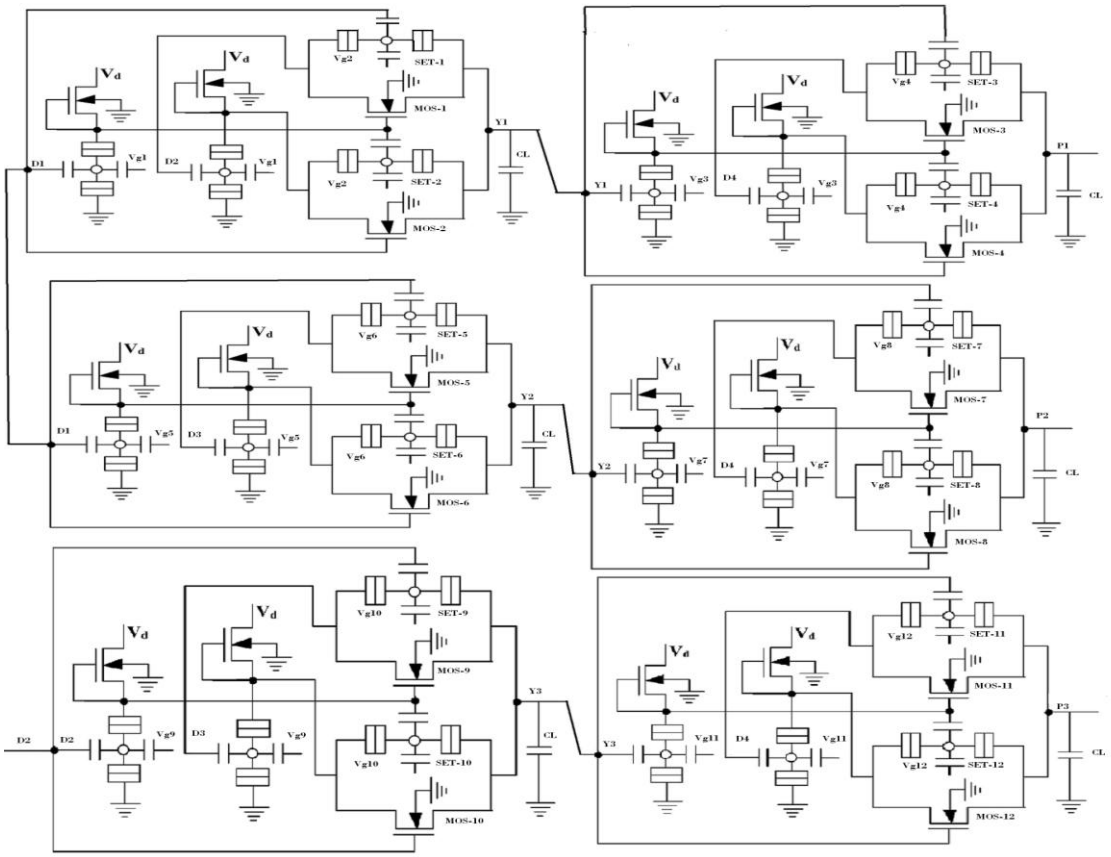

FIG.2: Hybrid Cmos-Set Hamming Code Nano Ic

Hybrid CMOS-SET circuit				
Circuit type	**Power supply**	**No of CMOS**	**No of SET**	**Power consumption**
NOT Gate	0.01v	6	6	$1.02e^{-09}$W
XOR Gate	0.01v	18	18	$1.02e^{-09}$W

Table 1: Comparative study of the SET and CMOS

IV. CONCLUSION

This paper examined the employment of SET-MOS hybrid logic gates based on single electron MOS transmission logic gates. From these results we can calculate the power dissipation of designed Hybrid CMOS-SET Hamming Code nano IC. The power dissipation and power supply voltage of Hybrid SET-MOS circuits are very low as designated in the table. PARTSIM simulator was used for simulation and the results showed greater tradeoff amid SET and CMOS. Here a step-wise procedure was followed. Computer simulation reveals that the designed circuits perform much better than the conventional CMOS made Hamming code IC. Thus the authors truly believe the next generation communication devices are to be designed using Hybrid CMOS-SET.

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